FD-SOI Transistors at Low Temperatures

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Abstract:

Introduction:

FD-SOI technology is an extremely attractive candidate for future low power and high speed electronic systems because it offers increased transconductance, decreased subthreshold slope, reduced short channel effects, elimination of kink effect and enhanced low field mobility[sherony]. It also offers niche applications, such as space exploration missions, radiation tolerance due to its small active volume[balestra]. These benefits have previously been demonstrated at room and high temperatures up to 350°C[ ].

Mission	Operating Temp.	Mission Temp.
Europa	-20 to +50° C	-170 to -50° C
Mars Sample Return	-40 to +50° C	-140 to +20° C
Pluto Flyby	-20 to +50° C	-235 to -100° C
Interstellar Tra	-20 to +50° C	-250 to -150° C
Champollion	-60 to +50° C	-150 to +20° C

Table 1. Operating and Mission Temperatures for Future Space Flight Missions

For most space applications, however, lower temperatures are often encountered. For the Europa Mission, the spacecraft will need to operate down to -125°C (148°K). In the past, the electronics in the spacecraft have been kept at device-friendly temperatures at the expense of high power consumption. As a result, devices that can operate reliably in harsh environments can provide valuable energy savings. For the commercial sector, low temperature operation of bulk devices have shown improved device characteristics such as higher current due to improved mobility[balestra, 95-9]. Our interest is to investigate whether FD-SOI transistor advantages are maintained, or even improved, at low temperatures.

Previous device performance measurements focused on partially-depleted SOI technologies with some FD-SOI devices [balestra, claeys]. Our reliability evaluation of FD-SOI technology for critical applications involve: variable temperature characterization of devices with different feature sizes (technology selection); long duration operation in critical environment (reliability assurance); and the effect of additional environmental factors such as radiation in addition to low the temperatures (overall reliability). We have completed the first phase of this evaluation process so far, with continuing work in order to complete all the three phases.

Body:

Experiments:

We have completed variable temperature measurements on FD-SOI transistors in the temperature range of 77°K to 300°K with device specifications given in Table 1 below. An HP4145 was used for automated current and voltage measurements. The temperature was cooled by running liquid nitrogen through a cryogenic (?) chamber. A cryostat maintained the temperature on the chuck that the device rested upon. Source-drain current (Ids), mobility, transconductance (Gm), voltage threshold (Vth), and the subthreshold slope are important parameters in the reliability and performance evaluation of the FD-SOI transistors. These parameters, examined at variable temperatures, are reported and discussed below.

Table 1. Device specifications:

Devices	Features	Si film thkns	Film doping	Tox thkns	BOX thnks	Width
FD-SOI Transistors	.25, .30, .35 μm	500 A	3.5 x 10^{17}/cc	75 A	1900 A	8 μm

Ids

Figure 1 shows the Ids behavior with respect to Vg at 77°K, 100°K, 150°K, 200°K, 250°K, and 300°K. We observed that as temperature decreases, the drain current increases _% from 300°K to 150°K. For comparison, the improvement in Ids from 0.35um to 025um is _%. Below 150°K, current started to decrease.

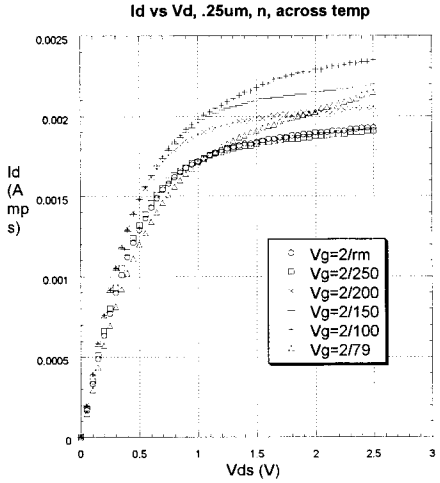

Figure 1. Id vs Vds for 0.25um transistor for temperature range of 77K to 300K.

Since the transistor Ids behavior is partly determined by the mobility, we next examine this parameter for explanations in the Ids curves.

Mobility

Mobility is expected to improve with decreasing temperature due to the decreasing lattice movement which allows electrons and holes to make it through the channel easier[Howe, Sodini]. Figure 2 shows our experimental data. Indeed, the results are as expected, at least down to 150°K.

Sorin Christoloveneau described a method of extracting effective mobility via the following equation:

$$\mu_{eff} = \frac{Id}{(W/L)QiVds}$$

Where $Qi = C_{ox}(V_g - V_t)$ [1, 4, 5] [Christoloveanu]

μ_{eff} is the effective mobility. This method is more accurate for experimental gate voltages in strong inversion. Figure 2 shows that the effective mobility increases with decreasing temperature when reasonably high gate voltages are applied.

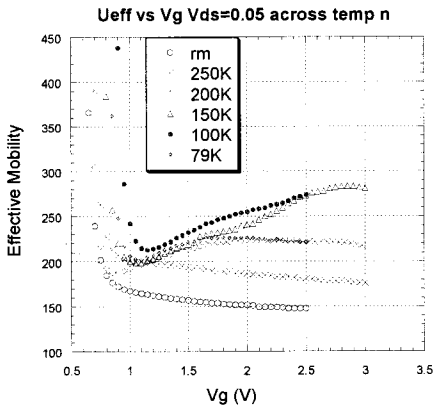

Figure 2. Effective Mobility vs. Gate Voltage for a Range of Temperatures for a 0.35um Transistor

Below 150K, we begin to observe impurity scattering[Steetman p.85-86]. This is when the mobility is no longer dominated by lattice scattering due to the thermal agitation of the lattice, but by the scattering caused by impurities when the carrier velocity slows down.

An interesting result is the variation of the effective mobility with channel length at a given temperature as shown in Figure 3. It is evident that the effective mobility is the highest for the 0.3 μm channel length transistor. The effective mobility is the same for both 0.25 and 0.35μm transistors.

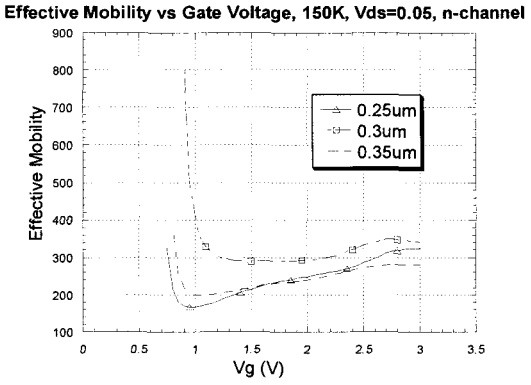

Figure 3. Mobility vs. Gate Voltage For Different Channel Lengths at 150K.

Transconductance

Transconductance is a measure of the channel mobility. Judging by the Ids and mobility behavior, we expect the transconductance to increase as well with decreasing temperature. Figure 4 illustrates this result from 300°K to 150°K. The decreasing trend below 100°K is, again, a reflection of the mobility behavior..

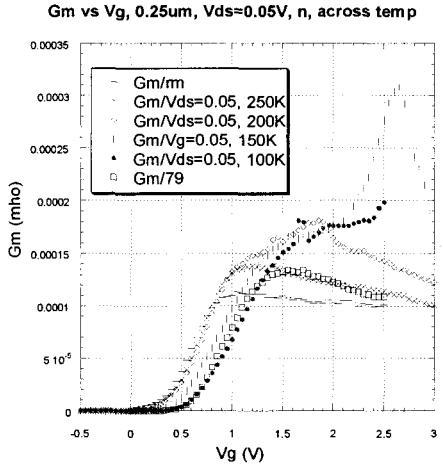

Figure 5. Transconductance vs. Gate Voltage for a 0.25um Transistor From Room Temperature Down to 79K.

Vth

Vth variation with temperature is a crucial parameter for device performance. We performed the voltage extraction by looking for the first peak of the d^2Id/dVg^2 curve[Sorin]. We observed, as shown in figure 5, that threshold voltage (Vth) increases with decreasing temperature in the range from 300°K to 100°K for all three channel lengths.

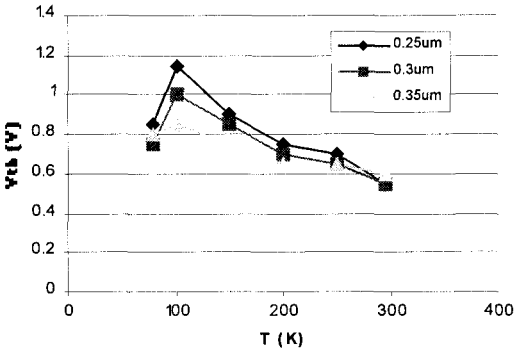

Figure 4. Vth vs. Temperature Plotted For Different Channel Length

This result seems to counter the Ids behavior. Higher Vth should lead to lower Ids. It is true this observation indicates higher leakage current below Vth and thus more power consumption, but in the end, the improvement in mobility was able to counter the Vth trend and yield an overall inversely proportional relationship between current and temperature.

Subthreshold Slope

The subthreshold slope (S) is a measure of the turn-on speed of the transistor. A smaller subthreshold slope indicates better performance. The relationship between S and temperature in the front channel is given as a first-order approximation by the equation:

$$S = 2.3\frac{kT}{q}\left(1 + \frac{Cit + Cd}{Cox}\right)$$ [Balestra]

Cit is interface trap equivalent capacitance. Cd is the depletion capacitance which does not

change with temperature. Figure 6 illustrates our observations. As expected, the subthreshold slope increases as temperature increasses. But the trend is not quite linear due to the Cit dependence on temperature as well

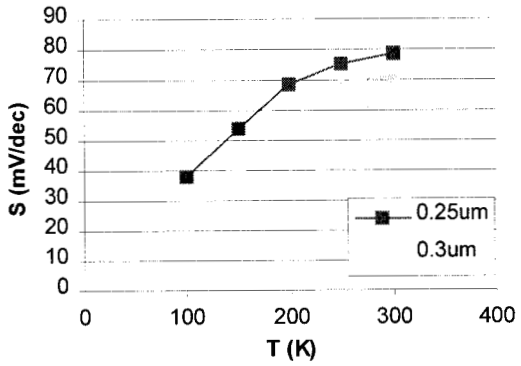

Figure 6. Subthreshold Slope vs. Temperature For 0.25um and 0.30um Transistors

Conclusion